Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A pipelined multistreaming processor, comprising:

an instruction ~~source~~cache having a plurality of ports~~:~~:

a first cluster of a plurality of instruction streams, said first cluster fetching instructions from ~~the~~ said instruction ~~source~~cache;

a second cluster of a plurality of instruction streams, said second cluster fetching instructions from ~~the~~ said instruction ~~source~~cache;

~~dedicated~~ a plurality of instruction queues, one for each of said instruction ~~for individual~~ streams in each of said first and second clusters;

a first ~~single~~ dispatch stage, coupled to said ~~dedicated to the~~ first cluster, ~~of streams~~ for dispatching to execution units instructions from ~~all of the~~ said instruction streams in ~~the~~ said first cluster ~~of streams to execution units~~; and

a ~~single~~ second dispatch stage, coupled to said ~~dedicated to the~~ second cluster, ~~of streams~~ for dispatching to execution units instructions from ~~all of the~~ said instruction streams in ~~the~~ said second cluster ~~of streams to execution units~~;

~~characterized in that the~~ wherein said first and second clusters operate independently, with ~~the dedicated~~ said first and second dispatch stages taking instructions only from ~~the~~ said plurality of instruction queues which are in ~~the individual~~ said clusters to which ~~the~~ said dispatch stages are dedicated; and

wherein said first and second clusters are coupled to said plurality of ports on said instruction cache, and can each utilize one or more of said plurality of ports.~~:~~

2. (Currently amended) The processor of claim 1 wherein individual ones or groups of said execution units are associated with and dedicated for use by ~~individual~~ either said first or second clusters.

3. (Currently amended) The processor of claim 1 wherein said individual streams in ~~a~~ said first cluster have dedicated fetch stages.

4. (Currently amended) The processor of claim 1 wherein the total number of said streams in the processor is eight, with four streams in each of said first and second clusters.

5. (Currently amended) The processor of claim 1 wherein instructions are fetched in each cycle for one of said instruction streams in each of said first and second clusters.

6. (Currently amended) The processor of claim 1 wherein ~~the~~ a set of fetch program counters (FPC) are monitored with one FPC dedicated to each of said instruction streams in each of said first and second clusters, and fetching of said instructions is directed beginning at addresses according to ~~the~~ said fetch program counters.

7. (Currently amended) The processor of claim ~~4~~ 1 wherein eight of said instructions are fetched for ~~a~~ one of said instruction streams each time instructions are fetched for that stream.

8. (Currently amended) The processor of claim ~~2~~ 1 further comprising one or more execution units coupled to said first and second dispatch stages to which either or both of said first and second dispatch stages may dispatch said instructions.

9. (Currently amended) In a pipelined multistreaming processor having an instruction ~~source~~ cache which has a plurality of ports, and a plurality of instruction streams executing within the processor, a method for ~~simplifying implementation and operation of the streams~~clustering ones of the plurality of instruction streams, comprising ~~the steps of~~:

~~(a)~~ clustering a first plurality of the instruction streams into ~~two or more clusters~~a first cluster;

clustering a second plurality of the instruction streams into a second cluster, the first and second plurality of the instruction streams being independent;

~~(b) dedicating~~ providing a ~~single~~ first dispatch stage to ~~all of~~ the first plurality of instruction streams of ~~each~~ the first cluster, for ~~dispatching~~ dispatching the first plurality of instructions to first execution units;

providing a second dispatch stage to the second plurality of instruction streams of the second cluster, for dispatching the second plurality of instructions to second execution units; and

~~(c)~~ in each cycle, fetching, ~~in each cycle, a series of~~ instructions from the instruction ~~source~~ cache ~~by a single cluster~~for one of the instruction streams in each of the first and second cluster.

10. (Currently amended) The method of claim 9 ~~further comprising~~wherein ~~groups of~~ a first plurality of execution units form the first execution units, and are dedicated to ~~each~~ the first cluster, and a second plurality of execution units form the second execution units, and are dedicated to the second cluster~~to which the dispatch stages in that cluster may dispatch instructions~~.

11. (Currently amended) The method of claim 9 ~~further comprising~~wherein said step of fetching utilizes fetch stages in each of the first and second clusters to fetch instructions for the instruction streams in each of the first and second clusters~~dedicated to individual streams in a cluster~~.

12. (Currently amended) The method of claim 9 wherein the total number of instruction streams in the processor is eight, and the number of instruction streams in each of the first and second clusters is four.

13. (Currently amended) The method of claim 9 having a fetch program counter (FPC) associated with each of the instruction streams, wherein said step of fetching is directed ~~beginning~~ at addresses according ~~to~~ within the fetch program counters.

14. (Currently amended) The method of claim 9 wherein in said step of fetching, eight instructions are fetched ~~each~~ each cycle for each of the first and second clusters~~time instructions are fetched for a stream~~.

15. (Currently amended) The method of claim 9 wherein the processor ~~further comprises~~ includes one or more general execution units, ~~and each dispatch stage is enabled to dispatch instructions to the general execution units~~coupled to both the first and second clusters, which may execute instructions dispatched from either or both of the first and second clusters.

16. (Currently amended) The method of claim 9 wherein each instruction stream in ~~each~~ the first and second clusters ~~has~~ have an instruction queue associated with ~~that stream~~them, and wherein the method further ~~comprising~~ comprises:

~~a step for~~ dispatching instructions ~~to execution units dedicated to each~~from the first and second clusters from the instruction queues associated with the instruction streams in ~~each~~ the first and second clusters.

17. (New) A processor for executing clusters of instruction threads, comprising:

an instruction cache for providing instructions to be executed, said instruction cache having a plurality of ports for simultaneously providing said instructions for a plurality of the instruction threads;

a first cluster, coupled to said instruction cache, said first cluster comprising:

at least one fetch stage, for fetching instructions for a first plurality of instruction threads within said first cluster;

a first plurality of instruction queues, coupled to said at least one fetch stage, for queuing instructions for each thread within said first plurality of instruction threads;

at least one dispatch stage, coupled to said plurality of instruction queues, for dispatching said instructions for execution; and

at least one execution unit, coupled to said at least one dispatch stage, for executing said instructions; and

a second cluster, coupled to said instruction cache, said second cluster comprising:

at least one fetch stage, for fetching instructions for a second plurality of instruction threads within said second cluster;

a second plurality of instruction queues, coupled to said at least one fetch stage, for queuing instructions for each thread within said second plurality of instruction threads;

at least one dispatch stage, coupled to said second plurality of instruction queues, for dispatching said instructions for execution; and

at least one execution unit, coupled to said at least one dispatch stage, for executing said instructions;

wherein said first cluster and said second cluster concurrently access said instruction cache.

18. (New) The processor as recited in claim 17 further comprising:

a general execution unit, coupled to both of said first and second cluster, for executing said instructions from both of said first and second clusters.

19. (New) The processor as recited in claim 17 wherein said at least one dispatch stage in each of said first and second clusters dispatches said instructions from said first and second plurality of instruction queues, for each of said threads within said instruction queues.

20. (New) The processor as recited in claim 17 further comprising:

a data cache, coupled to each of said first and second cluster, for providing data to be operated on by each of said instruction threads in each of said clusters.